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A strategic scheme of quantum Monte Carlo implementation bringing out the potential in a supercomputer with many-core processors

Quantum annealing (QA) is a promising algorithm to solve combinatorial optimization problems with high efficiency [1,2]. Since the appearance of commercial quantum annealing processor, some hardware based on the Ising model to solve combinatorial optimization problems has been proposed and developed exhaustively. On the contrary, we considered a method to accelerate the parallel computation in quantum Monte Carlo (QMC) simulations. A QMC algorithm can treat QA in conventional classical computers toward the realization of high-performance computation of large-scale combinatorial optimization problems. We implemented a QMC algorithm on many-core processors, PEZY-SCs. PEZY-SC is a Multiple Instruction/Multiple Data (MIMD) processor with 1024 computing cores, in which eight threads run independently. In this architecture, by using the core-local memory and synchronization, the communications between the threads in a core are much faster than the global communications. Since QMC is implemented by using the Suzuki-Trotter decomposition [3,4], it can be regarded as a pseudo-parallelization calculation [5] in which the interactions in the imaginary-time direction exist. Thus, it is reasonable to assign the whole trotters of a spin (qubit) to the same core (i.e. eight threads). Furthermore, the MIMD feature of PEZY-SC is suited for an efficient calculation since the interactions between spins are inhomogeneous in combinatorial optimization problems. The communication between multiple processors is performed by Message Passing Interface (MPI), which can share the state of spins. To estimate the efficiency of the scaling of multiprocessors, we measured the performance of QMC on PEZY-SC depending on the problem size. Here, we assumed that the connections, i.e., the interactions between spins in the real space, are sparse as well as the Chimera graph that D-Wave Systems Inc. adopted. Our result suggests that when the number of spins is not so large, it is effective to retain all spins within a processor since the communications between processors require a certain amount of overhead for data exchange and synchronization. While when the number of spins grows, the advantage of multiple processors comes out.

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