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An Architecture for Parallel-Trial Hardware Accelerator for Ising-Model MCMC Search

We developed an architecture for parallel-trial hardware that minimizes the energy of Ising models, and implemented it in a system using an FPGA. The system can handle Ising models with 1,024 state variables forming a complete graph connected through 16-bit fixed-point signed binary weights. The bias terms (i.e., the values of the external field) in the Ising model are expressed in 26-bit signed binary and configurable for each bit. The system uses an accelerator engine that performs a Markov-chain Monte-Carlo search with a parallel evaluation of the energy increment prior to selection of a single state variable to be flipped, achieving a speedup while guaranteeing a convergence. The engine is implemented in Arria 10 GX FPGA and solved 32-city traveling salesman problems 12,000 times faster than a simulated annealing running on a 3.5-GHz Intel Xeon E5-1620v3 processor.

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