A fine-grain digit-serial multiple-valued reconfigurable VLSI is proposed for effective use of the hardware resources. Resource sharing allocation where one or more nodes in a control/data flow graph are mapped into a single arithmetic/logic circuit makes it possible to reduce the number of the arithmetic/logic circuits. In the resource sharing allocation, control and the arithmetic/logic circuits are constructed by using one or multiple cells, where a cell consists of a logic block and switch block. In the logic-in-control architecture, only one state in a state transition diagram is allocated to one cell to implement the control circuit, which leads to reduction of the complexity of interconnections between cells. A 3-variable binary operation is required for implementing the control circuit, and the hardware resource is shared as a common hardware resource for the arithmetic/logic circuit to make the high utilization ratio of the cell. The fine-grain cell is implemented based on multiple-valued current-mode circuit technology. Multiple-valued signal transfer between cells and a linear summation just by wiring are effectively employed for reduction of the area of the cell.